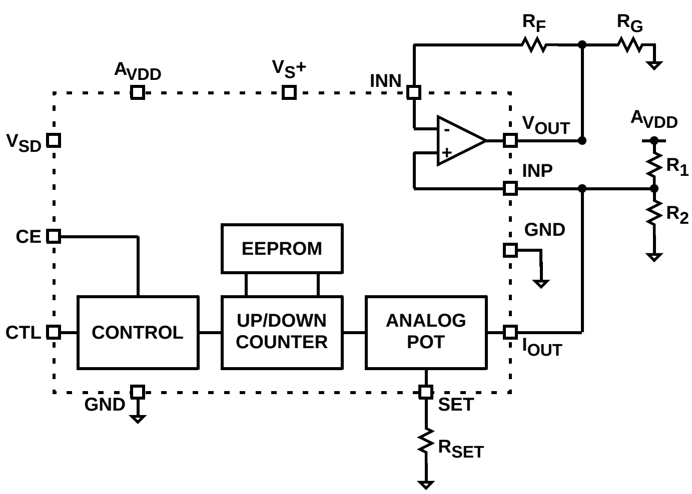
Data Sheet October 30, 2008 FN7438.1

Programmable V_{COM}

The EL9200, EL9201, and EL9202 represent programmable V_{COM} amplifiers for use in TFT-LCD displays. Featuring 1, 2, and 4 channels of V_{COM} amplification, respectively, each device features just a single programmable current source for adding offset to one V_{COM} output. This current source is programmable using a single wire interface to one of 128 levels. The value is stored on an internal EEPROM memory.

The EL9200 is available in the 12 LD DFN package and the EL9201 and EL9202 are available in 24 LD QFN packages. All are specified for operation over the -40°C to +85°C temperature range.

Typical Block Diagram



Features

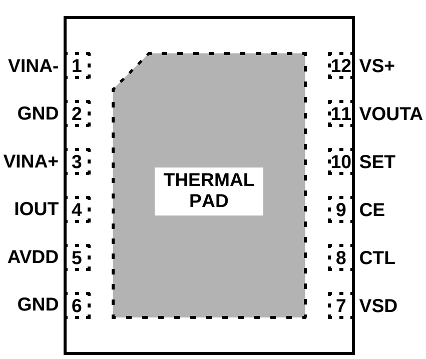
- 128 Step Adjustable Sink Current
- EEPROM Memory
- 2-pin Adjustment and Disable
- Single, Dual or Quad Amplifiers
  - 44MHz Bandwidth
  - 80V/µs Slew Rate
  - 60mA Continuous Output
  - 180mA Peak Output
- Up to 18V Operation
- 2.6V to 3.6VLogic Control
- Pb-free Available (RoHS compliant)

Applications

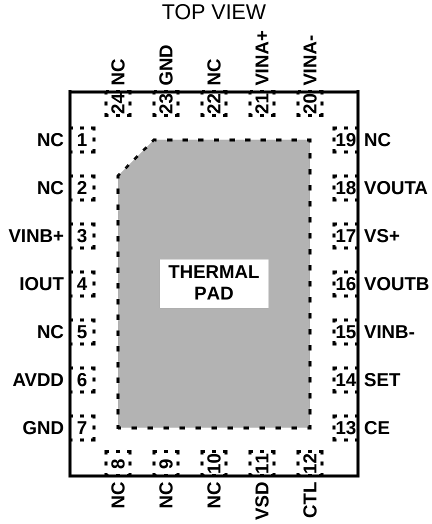
- TFT-LCD V_{COM} Supplies For
  - LCD-TVs
  - LCD Monitors

Pinouts

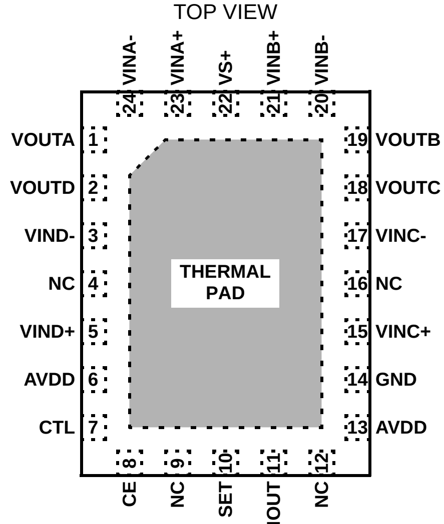
EL9200
(12 LD DFN)
TOP VIEW



EL9201
(24 LD QFN)
TOP VIEW



EL9202
(24 LD QFN)
TOP VIEW



Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
EL9200IL	9200IL	-40 to +85	12 LD DFN	L12.4x4B
EL9200IL-T7*	9200IL	-40 to +85	12 LD DFN	L12.4x4B
EL9200IL-T13*	9200IL	-40 to +85	12 LD DFN	L12.4x4B
EL9200ILZ (Note)	9200ILZ	-40 to +85	12 LD DFN (Pb-Free)	L12.4x4B
EL9200ILZ-T7* (Note)	9200ILZ	-40 to +85	12 LD DFN (Pb-Free)	L12.4x4B
EL9200ILZ-T13* (Note)	9200ILZ	-40 to +85	12 LD DFN (Pb-Free)	L12.4x4B
EL9201IL	9201IL	-40 to +85	24 LD QFN	MDP0046
EL9201IL-T7*	9201IL	-40 to +85	24 LD QFN	MDP0046
EL9201IL-T13*	9201IL	-40 to +85	24 LD QFN	MDP0046
EL9201ILZ (Note)	9202ILZ	-40 to +85	24 LD QFN (Pb-Free)	MDP0046
EL9201ILZ-T7* (Note)	9202ILZ	-40 to +85	24 LD QFN (Pb-Free)	MDP0046
EL9201ILZ-T13* (Note)	9202ILZ	-40 to +85	24 LD QFN (Pb-Free)	MDP0046
EL9202IL	9202IL	-40 to +85	24 LD QFN	MDP0046
EL9202IL-T7*	9202IL	-40 to +85	24 LD QFN	MDP0046
EL9202IL-T13*	9202IL	-40 to +85	24 LD QFN	MDP0046
EL9202ILZ (Note)	9202ILZ	-40 to +85	24 LD QFN (Pb-Free)	MDP0046
EL9202ILZ-T7* (Note)	9202ILZ	-40 to +85	24 LD QFN	MDP0046
EL9202ILZ-T13* (Note)	9202ILZ	-40 to +85	24 LD QFN (Pb-Free)	MDP0046

*Add "-T" suffix for tape and reel *Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = +25°C)

V_S+ Supply Voltage between V_S+ and GND 18V
Supply Voltage between V_{SD} and GND 4V
Maximum Continuous Output Current 65mA
Input Voltages to GND
SET, CE . . . .-0.3V to +4V
CTL. . . . .-0.3V to +16V
Output Voltages to GND
OUT . . . .-0.3V to +20V
A_{VDD} . . . .-0.3V to +20V
ESD Rating
Human Body Model 2kV

Thermal Information

Maximum Die Temperature . . . . +150°C
Storage Temperature . . . .-65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Operating Temperature . . . .-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_{SD} = 3V, V_S+ = 15V, A_{VDD} = 15V, R_{SET} = 24.9kΩ, and T_A = +25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
V_{S+}	Supply Voltage		4.5		16.5	V
I_{S+}	Quiescent Current	EL9200		3.8	4.8	mA
		EL9201		7.6	9.6	mA
		EL9202		10.5	16	mA
V_{SD}	Logic Supply Voltage	For programming	3		3.6	V
		For operation	2.6		3.6	V
I_{SD}	Quiescent Logic Current	CE = 3.6V			50	µA
		CE = GND			25	µA
		Program (charge pump current) (Note 1)			23	mA
		Read (Note 1)			3	mA
I_{ADD}	Supply Current	(Note 2)			25	µA
CTL_{IH}	CTL High Voltage	2.6V < V_{SD} < 3.6V	0.7*V_{SD}		0.8*V_{SD}	V
CTL_{IL}	CTL Low Voltage	2.6V < V_{SD} < 3.6V	0.2*V_{SD}		0.3*V_{SD}	V
CTL_{IHRPW}	CTL High Rejected Pulse Width		20			µs
CTL_{ILRPW}	CTL Low Rejected Pulse Width		20			µs
CTL_{IHMPW}	CTL High Minimum Pulse Width		200			µs
CTL_{ILMPW}	CTL Low Minimum Pulse Width				200	µs
CTL_{MTC}	CTL Minimum Time Between Counts			10		µs
ICTL	CTL Input Current	CTL = GND			10	µA
		CTL = V_{SD}			10	µA
CTL_{CAP}	CTL Input Capacitance			10		pF
CE_{IL}	CE Input Low Voltage	2.6V < V_{SD} < 3.6V			0.4	V
CE_{IH}	CE Input High Voltage	2.6V < V_{SD} < 3.6V	1.6			V
CE_{ST}	CE Minimum Start-Up Time	(Note 1)	1			ms
CTL_{PROM}	CTL EEPROM Program Voltage	2.6V < V_{SD} < 3.6V (Note 2)	4.9		15.75	V
CTL_{PT}	CTL EEPROM Programming Signal Time	> 4.9V	200			µs
P_T	Programming Time			100		ms
EE_{WC}	EE Write Cycles	(Note 5)	1000			cycles

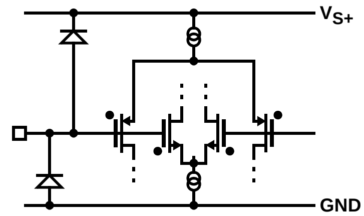
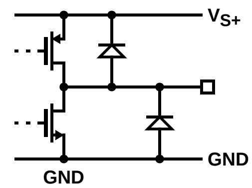
Electrical Specifications V_{SD} = 3V, V_S+ = 15V, A_{VDD} = 15V, R_{SET} = 24.9kΩ, and T_A = +25°C unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
SET_{DN}	SET Differential Nonlinearity	Monotonic over-temperature		±1		LSB
SET_{ZSE}	SET Zero-Scale Error	(Note 3)			±2	LSB
SET_{FSE}	SET Full-Scale Error	(Note 3)			±8	LSB
I_{SET}	SET Current	Through R_{SET} (Note 1)			120	µA
SET_{ER}	SET External Resistance	To GND, A_{VDD} = 20V (Note 1)	10		200	kΩ
		To GND, A_{VDD} = 4.5V (Note 1)	2.25		45	kΩ
A_{VDD} to SET	A_{VDD} to SET Voltage Attenuation			1:20		V/V
OUT_{ST}	OUT Settling Time	To ±0.5 LSB error band (Note 1)		20		µs
V_{OUT}	OUT Voltage Range	(Note 1)	V_{SET} + 0.5V		13	V
OUT_{VD}	OUT Voltage Drift	(Note 1)			10	mV
AMPLIFIER CHARACTERISTICS						
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 1)			7		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	60	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMRR	Common-Mode Rejection Ratio	For V_{IN} from -5.5V to +5.5V	50	70		dB
A_{VOL}	Open-Loop Gain	-4.5V ≤ V_{OUT} ≤ +4.5V	60	70		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	R_L = 1.5kΩ to 0		0.09	0.15	V
V_{OH}	Output Swing High		14.85	14.9		V
I_{SC}	Short-Circuit Current		±150	±180		mA
I_{OUT}	Output Current			±65		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_{S+} is moved from 4.5V to 15.5V	55	80		dB
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 4)	-4.0V ≤ V_{OUT} ≤ 4.0V, 20% to 80%	60	80		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_{OUT} = 2V step		80		ns
BW	-3dB Bandwidth			44		MHz
GBWP	Gain-Bandwidth Product			32		MHz
PM	Phase Margin			50		°
CS	Channel Separation	f = 5MHz (EL9201 and EL9202 only)		110		dB
d_G	Differential Gain (Note 5)	R_F = R_G = 1kΩ and V_{OUT} = 1.4V		0.17		%
d_P	Differential Phase (Note 5)	R_F = R_G = 1kΩ and V_{OUT} = 1.4V		0.24		°

NOTES:

1. Simulated and determined via design and not directly tested
2. Tested at A_{VDD} = 20V
3. Wafer sort only
4. NTSC signal generator used
5. Limits established by characterization and are not production tested.

Pin Descriptions

PIN	IN/OUT	DESCRIPTION	EQUIVALENT CIRCUIT
VINx-	Input	Amplifier x inverting input, where: x = A for EL9200 x = A, B for EL9201 x = A, B, C, D for EL9202	 CIRCUIT 1
VINx+	Input	Amplifier x non-inverting input, where: x = A for EL9200 x = A, B for EL9201 x = A, B, C, D for EL9202	Reference Circuit 1
VS+	Supply	Op amp supply; bypass to GND with 0.1µF capacitor	
VOUTX	Output	Amplifier X output, where: x = A for EL9200 x = A, B for EL9201 x = A, B, C, D for EL9202	 CIRCUIT 2
NC	-	No connect; not internally connected	
GND	Supply	Ground connection	
IOUT	Output	Adjustable sink current output pin; the current sinks into the OUT pin is equal to the DAC setting times the maximum adjustable sink current divided by 128; see SET pin function description for the maxim adjustable sink current setting	
SET	Output	Maximum sink current adjustment point; connect a resistor from SET to GND to set the maximum adjustable sink current of the OUT pin; the maximum adjustable sink current is equal to (A_{VDD}/20) divided by R_{SET}	
CE	Input	Counter enable pin; connect CE to V_{DD} to enable counting of the internal counter; connect CE to GND to inhibit counting	
CTL	Input	Internal counter up/down control and internal EEPROM programming control input; if CE is high, a mid-to-low transition increments the 7-bit counter, raising the DAC setting, increasing the OUT sink current, and lowering the divider voltage at OUT; a mid-to-high transition decrements the 7-bit counter, lowering the DAC setting, decreasing the OUT sink current, and increasing the divider voltage at OUT; applying 4.9V and above with appropriately arranged timing will overwrite EEPROM with the contents in the 7-bit counter; see EEPROM Programming section for details	
AVDD	Supply	Analog voltage supply; bypass to GND with 0.1µF capacitor	
VSD	Supply	System power supply input; bypass to GND with 0.1µF capacitor	

Amplifier Typical Performance Curves

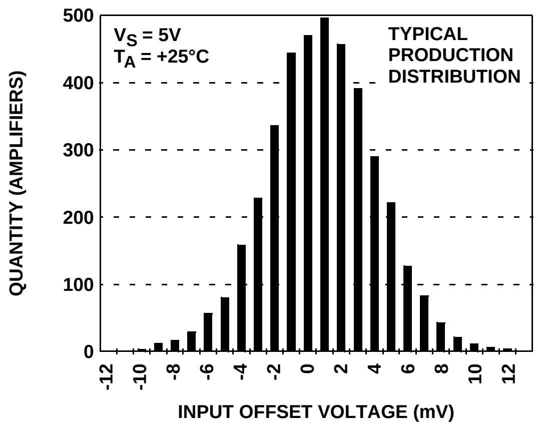


FIGURE 1. INPUT OFFSET VOLTAGE DISTRIBUTION

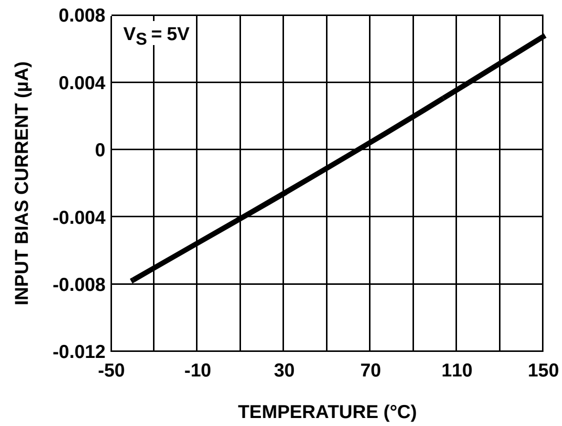


FIGURE 2. INPUT BIAS CURRENT vs TEMPERATURE

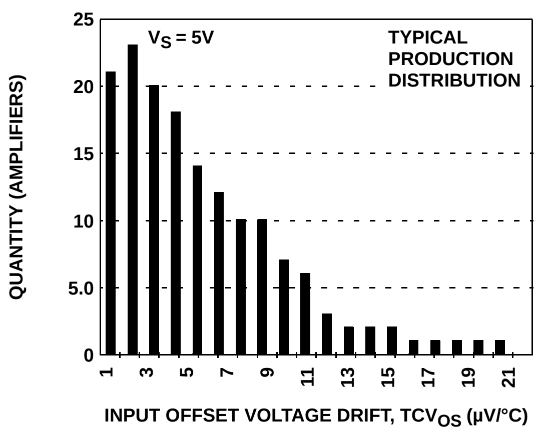


FIGURE 3. INPUT OFFSET VOLTAGE DRIFT

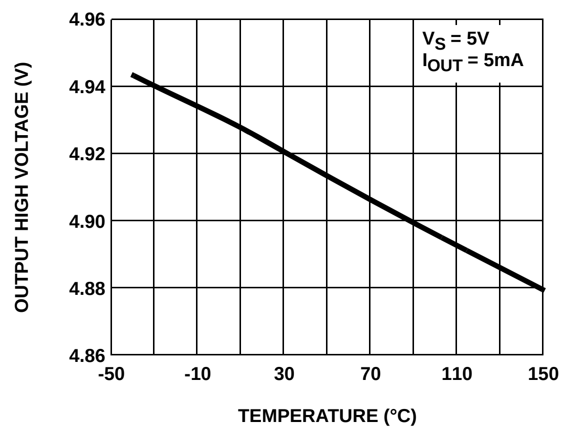


FIGURE 4. OUTPUT HIGH VOLTAGE vs TEMPERATURE

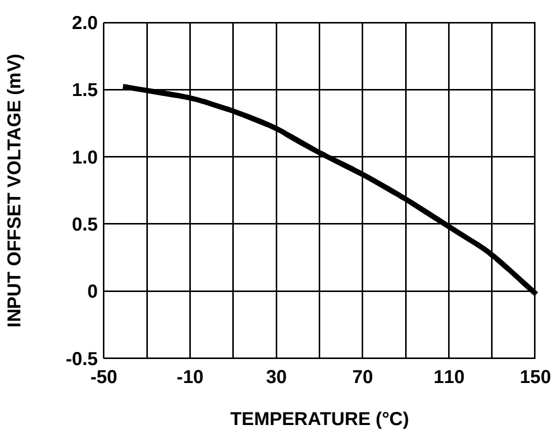


FIGURE 5. INPUT OFFSET VOLTAGE vs TEMPERATURE

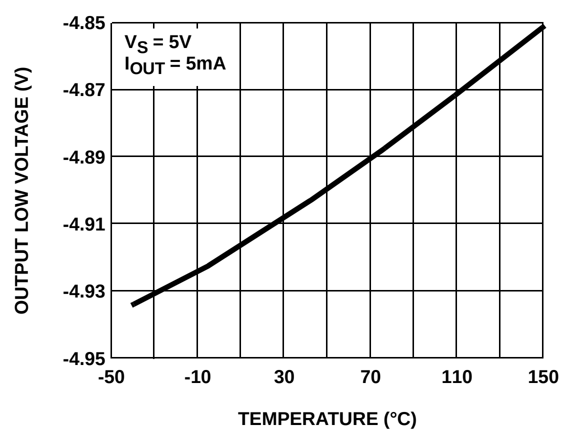


FIGURE 6. OUTPUT LOW VOLTAGE vs TEMPERATURE

Amplifier Typical Performance Curves (Continued)

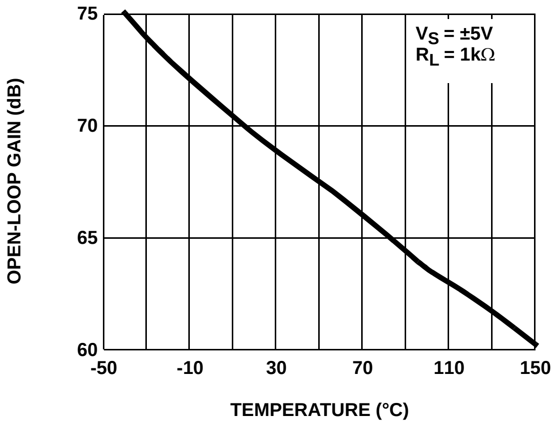


FIGURE 7. OPEN-LOOP GAIN vs TEMPERATURE

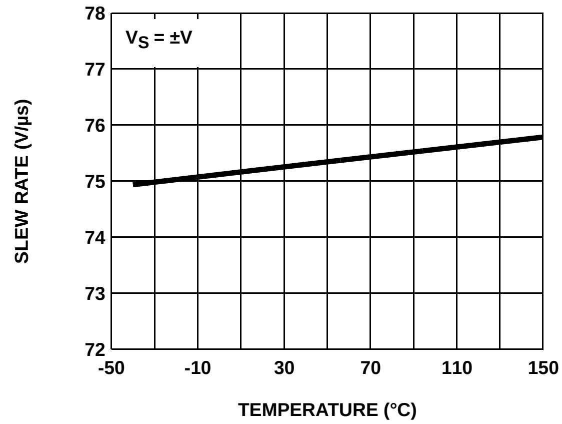


FIGURE 8. SLEW RATE vs TEMPERATURE

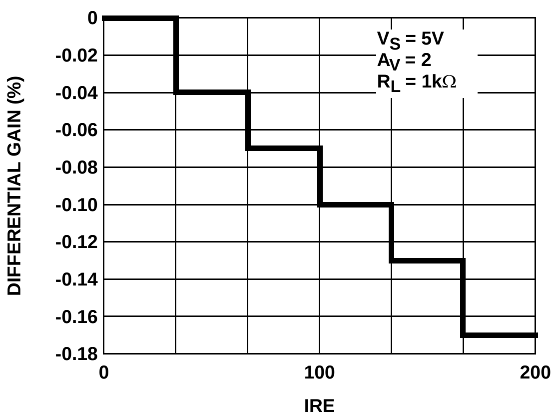


FIGURE 9. DIFFERENTIAL GAIN

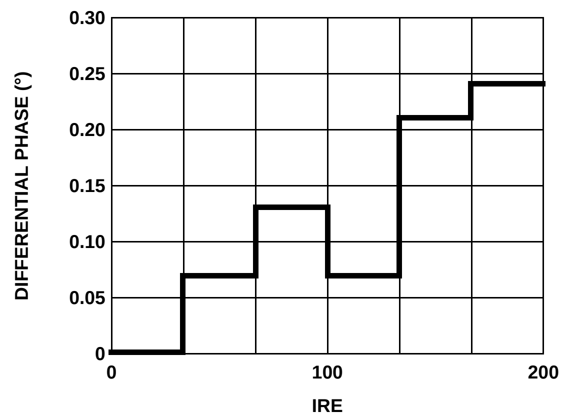


FIGURE 10. DIFFERENTIAL PHASE

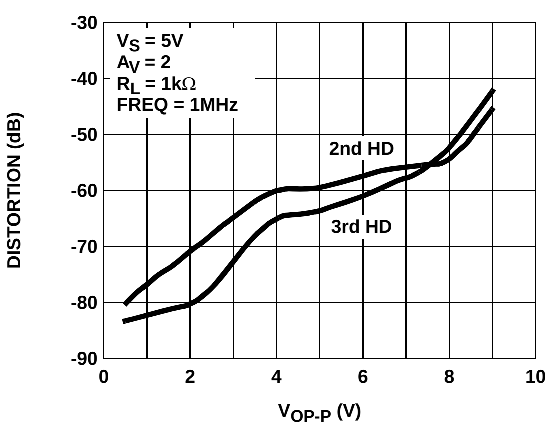


FIGURE 11. HARMONIC DISTORTION vs V_{OP-P}

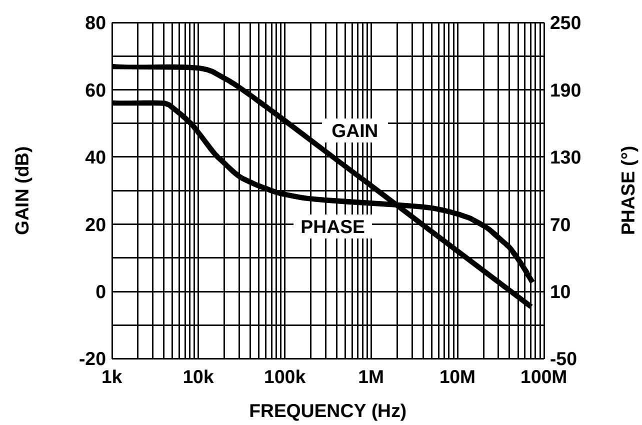


FIGURE 12. OPEN LOOP GAIN AND PHASE

Amplifier Typical Performance Curves (Continued)

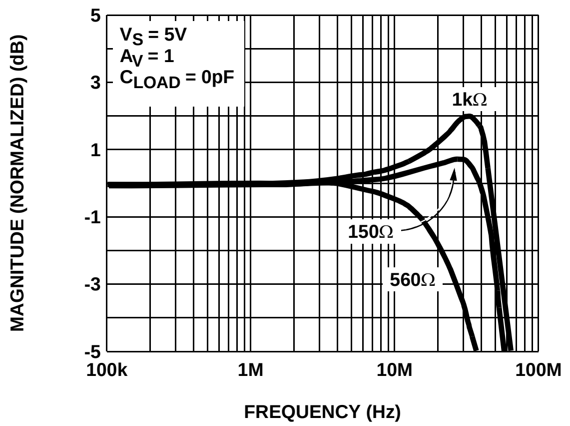


FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS R_L

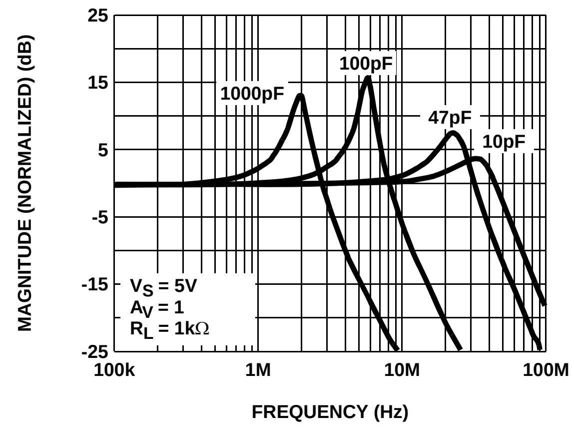


FIGURE 14. FREQUENCY RESPONSE FOR VARIOUS C_L

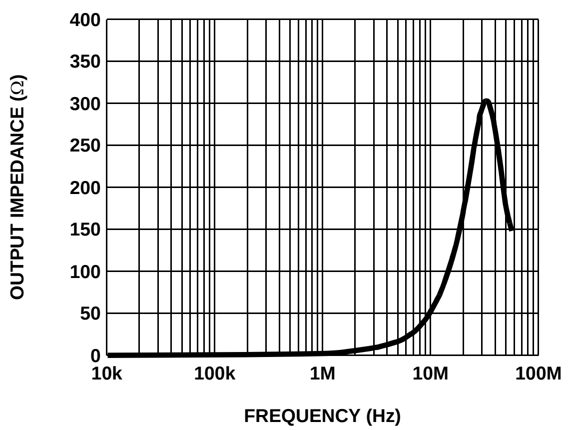


FIGURE 15. CLOSED LOOP OUTPUT IMPEDANCE

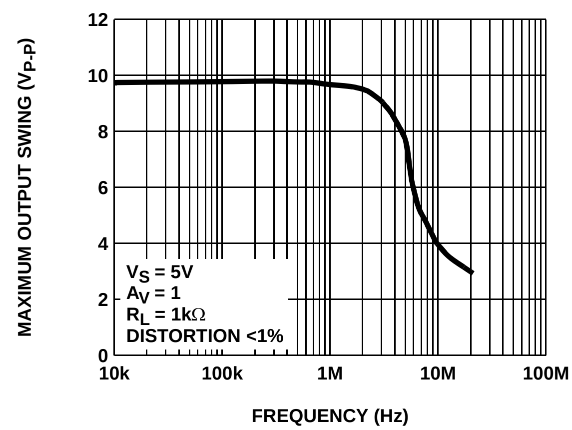


FIGURE 16. MAXIMUM OUTPUT SWING vs FREQUENCY

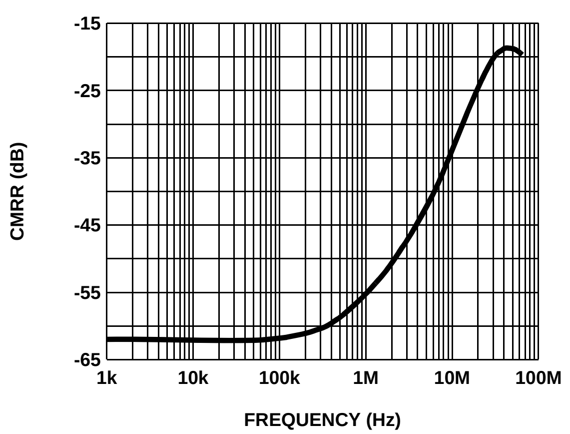


FIGURE 17. CMRR

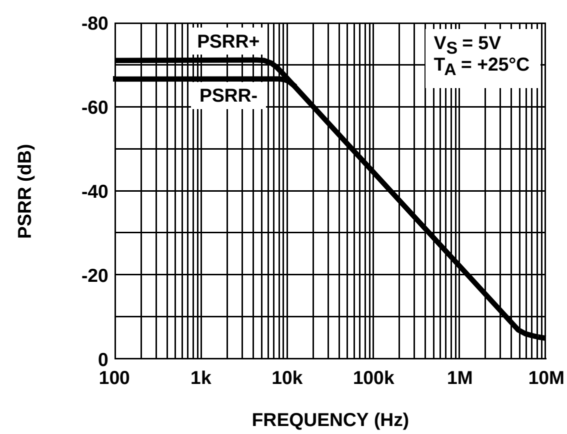


FIGURE 18. PSRR

Amplifier Typical Performance Curves (Continued)

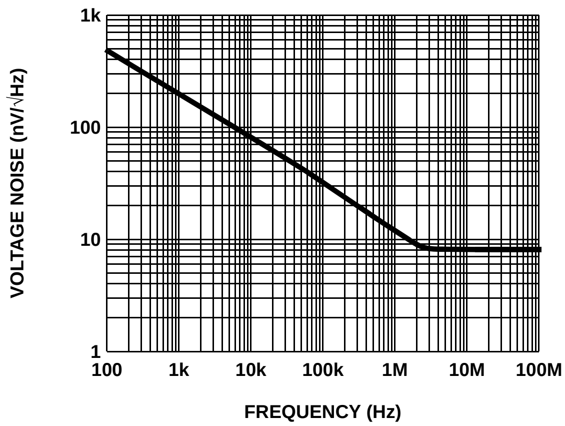


FIGURE 19. INPUT VOLTAGE NOISE SPECTRAL DENSITY

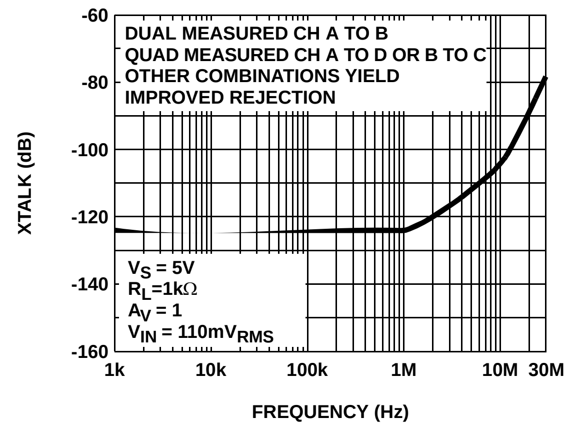


FIGURE 20. CHANNEL SEPARATION

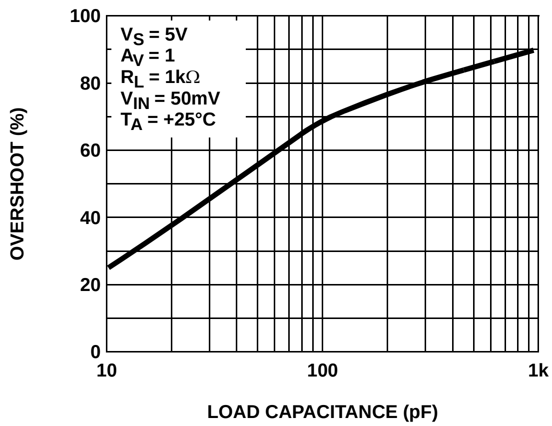


FIGURE 21. SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

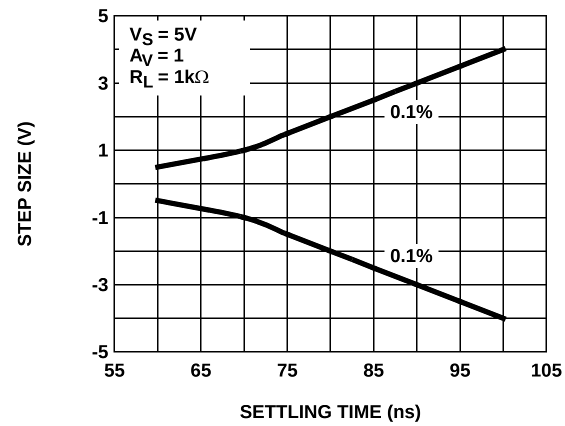


FIGURE 22. SETTLING TIME vs STEP SIZE

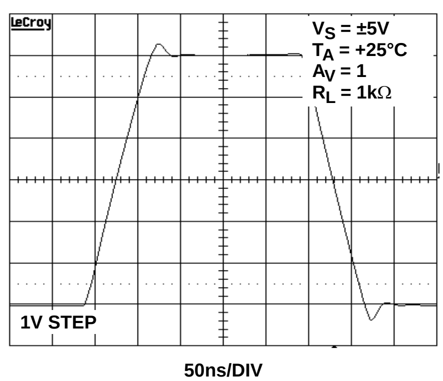


FIGURE 23. LARGE SIGNAL TRANSIENT RESPONSE

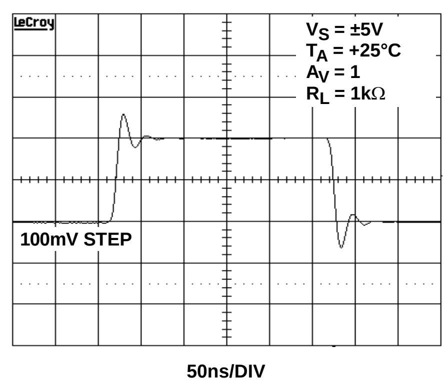


FIGURE 24. SMALL SIGNAL TRANSIENT RESPONSE

Amplifier Typical Performance Curves (Continued)

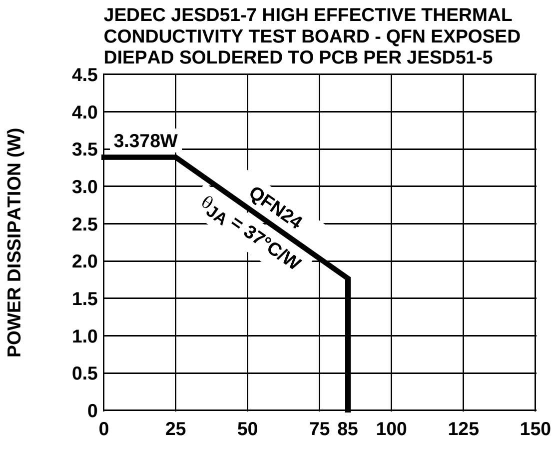


FIGURE 25. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

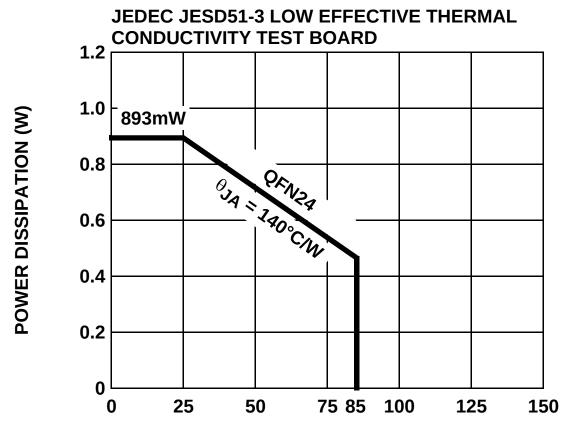


FIGURE 26. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Application Information

This device provides the ability to reduce the flicker of an LCD panel by adjustment of the V_{COM} voltage during production test and alignment. A 128-step resolution is provided under digital control which adjusts the sink current of the output. The output is connected to an external voltage divider, so that the device will have the capability to reduce the voltage on the output by increasing the output sink current.

The adjustment of the output and the programming of the non-volatile memory are provided on one pin while the counter enable (CE) is provided on a separate pin. The output is adjusted via the CTL pin either by counting up with a mid to low transition or by counting down with a mid to high transition. Once the minimum or maximum value is reached on the 128 steps, the device will not overflow or underflow beyond that minimum or maximum value. An increment of the counter will increase the output sink current which will lower the voltage on the external voltage divider. A decrement of the counter will decrease the output sink current, which will raise the voltage on the external voltage divider.

Once the desired output level is obtained, the part can store it's setting using the non-volatile memory in the device. See the “Non-Volatile Memory (EEPROM) Programming” on page 12 for detailed information.

Note: Once the desired output level is stored in the EEPROM, the CE pin must go low to preserve the stored value.

Adjustable Sink Current Output

The device provides an output sink current which lowers the voltage on the external voltage divider. The equations that control the output are given in Equation 1:

$$I_{OUT} = \frac{Setting}{128} \times \frac{A_{VDD}}{20(R_{SET})}$$

$$V_{OUT} = \left(\frac{R_2}{R_1 + R_2}\right) V_{AVDD}\left(1 - \frac{Setting}{128} \times \frac{R_1}{20(R_{SET})}\right) \quad \text{(EQ. 1)}$$

NOTE: Where setting is an integer between 1 and 128.

7-Bit Up/Down Counter

The counter sets the level to the digital potentiometer and is connected to the non-volatile memory. When the part is programmed, the counter setting is loaded into the non-volatile memory. This value will be loaded from the non-volatile memory into the counter during power-on. The counter will not exceed its maximum level and will hold that value during subsequent increment requests on the CTL pin. The counter will not exceed its minimum level and will hold that value during subsequent decrement requests on the CTL pin.

CTL Pin

CTL should have a noise filter to reduce bouncing or noise on the input that could cause unwanted counting when the CE pin is high. The board should have an additional ESD protection circuit, with a series 1kΩ resistor and a shunt 0.01µF capacitor connected on the CTL pin.

In order to increment the setting, pulse CTL low for more than 200µs. The output sink current increases and lowers the V_{COM} lever by one least-significant bit (LSB). On the other hand, to decrement the setting, pulse CTL high for more than 200µs. The output sink current will decrease and the V_{COM} level will increase by one LSB.

To avoid unintentional adjustment, the EL9200, EL9201, and EL9202 guarantees to reject CTL pulses shorter than 20µs.

Since the internal comparators come up in an unknown state, the very first CTL pulse is ignored to avoid the possibility of a false pulse.

See Figure 27 for the timing information.

TABLE 1. TRUTH TABLE

INPUT			OUTPUT		
CTL	**CE**	**V_{DD}**	**SET**	**I_{CC}**	**MEMORY**
Mid to Hi	Hi	V_{DD}	Decrement	Normal	X
Mid to Lo	Hi	V_{DD}	Increment	Normal	X
X	Lo	V_{DD}	No Change	Lower	X
> 4.9V	X	V_{DD}	No Change	Increased	Program
X	X	0 to V_{DD}	Read	Increased	Read

NOTE: CE should be disabled (pulled low) before powering down the device to assure that the glitches and transients will not cause unwanted EEPROM overwriting.

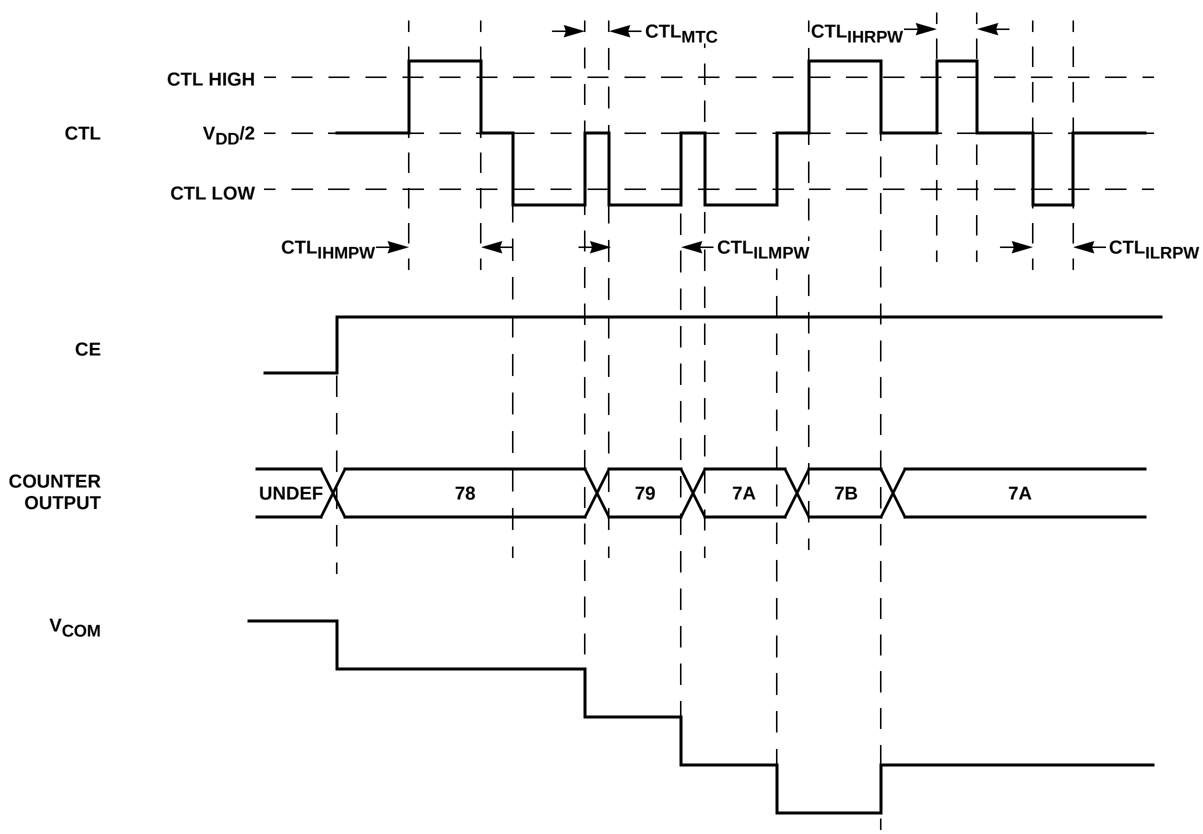


FIGURE 27. V_{COM} ADJUSTMENT

Non-Volatile Memory (EEPROM) Programming

When the CTL pin exceeds 4.9V, the non-volatile programming cycle will be activated. The CTL signal needs to remain above 4.9V for more than 200µs. The level and timing needed to program the non-volatile memory is given below. It then takes a maximum of 100ms for the programming to be completed inside the device (see P_T specification in Table Electrical Specifications on page 3.

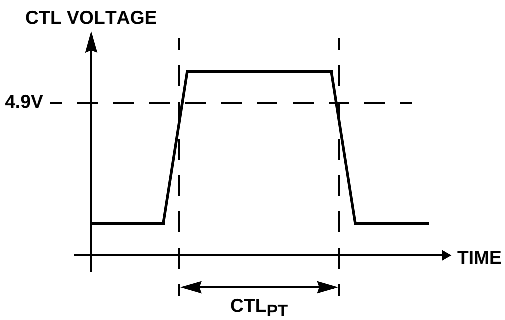


FIGURE 28. EEPROM PROGRAMMING

Amplifiers' Operating Voltage, Input, and Output

The amplifiers are specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range of 4.5V to 16.5V. Most amplifier specifications are stable over both the full supply range and operating temperatures of -40°C to +85°C. Parameter variations with operating voltage and/or temperature are shown in the See "Amplifier Typical Performance Curves" on page 6.

The input common-mode voltage range of the amplifiers extends 500mV beyond the supply rails. The output swings of the those typically extend to within 100mV of positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 27 shows the input and output waveforms for the device in the unity-gain configuration. Operation is from 5V supply with a 1kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid. The output voltage is approximately $9.8V_{P-P}$.

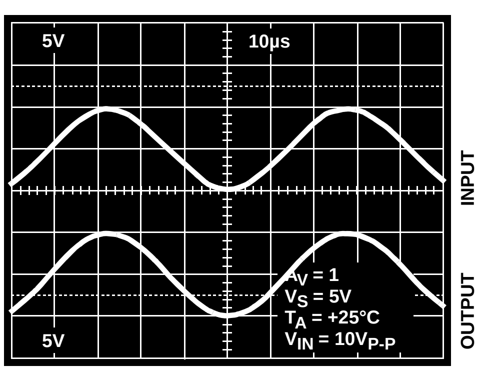


FIGURE 29. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT

Short-Circuit Current Limit

The amplifiers will limit the short circuit current to ±180mA if the output is directly shorted to the positive or the negative supply. If an output is shorted indefinitely, the power dissipation could easily increase such that the device may be damaged. Maximum reliability is maintained if the output continuous current never exceeds ±65mA. This limit is set by the design of the internal metal interconnects.

Output Phase Reversal

The amplifiers are immune to phase reversal as long as the input voltage is limited from V_S- -0.5V to V_S+ +0.5V. Figure 28 shows a photo of the output of the device with the input voltage driven beyond the supply rails. Although the device's output will not change phase, the input's overvoltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diodes placed in the input stage of the device begin to conduct and over-voltage damage could occur.

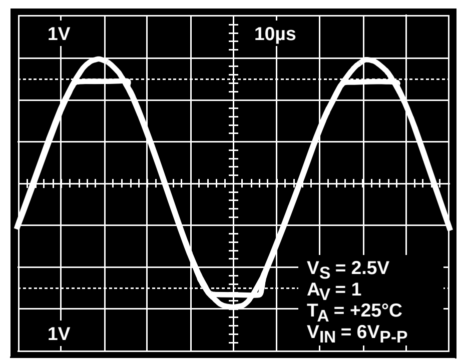


FIGURE 30. OPERATION WITH BEYOND-THE-RAILS INPUT

Unused Amplifiers

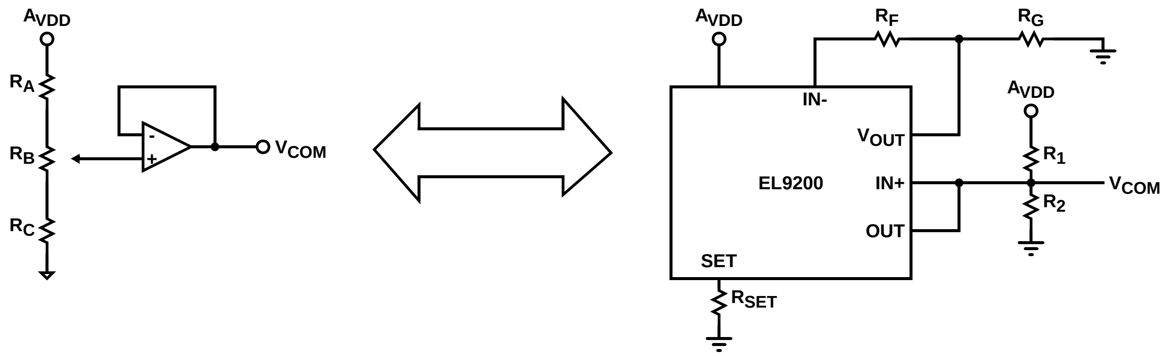
It is recommended that any unused amplifiers in a dual and a quad package be configured as a unity gain follower. The inverting input should be directly connected to the output and the non-inverting input tied to the ground plane.

Power Supply Bypassing and Printed Circuit Board Layout

The amplifiers can provide gain at high frequency. As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal operation, a 0.1µF ceramic capacitor should be placed from V_S to pin to GND. A 4.7µF tantalum capacitor should then be connected in parallel, placed in the region of the amplifier.

Replacing Existing Mechanical Potentiometer Circuits

Figures 29 and 30 show the common adjustment mechanical circuits and equivalent replacement with the EL920x.

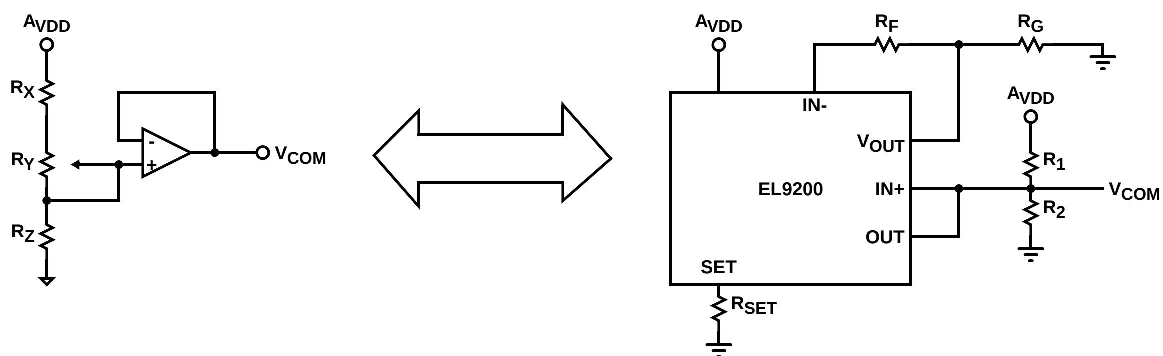


$$R_1 = R_A$$

$$R_2 = R_B + R_C$$

$$R_{SET} = \frac{R_A(R_B + R_C)}{20R_B}$$

FIGURE 31. EXAMPLE OF THE REPLACEMENT FOR THE MECHANICAL POTENTIOMETER CIRCUIT USING EL9200



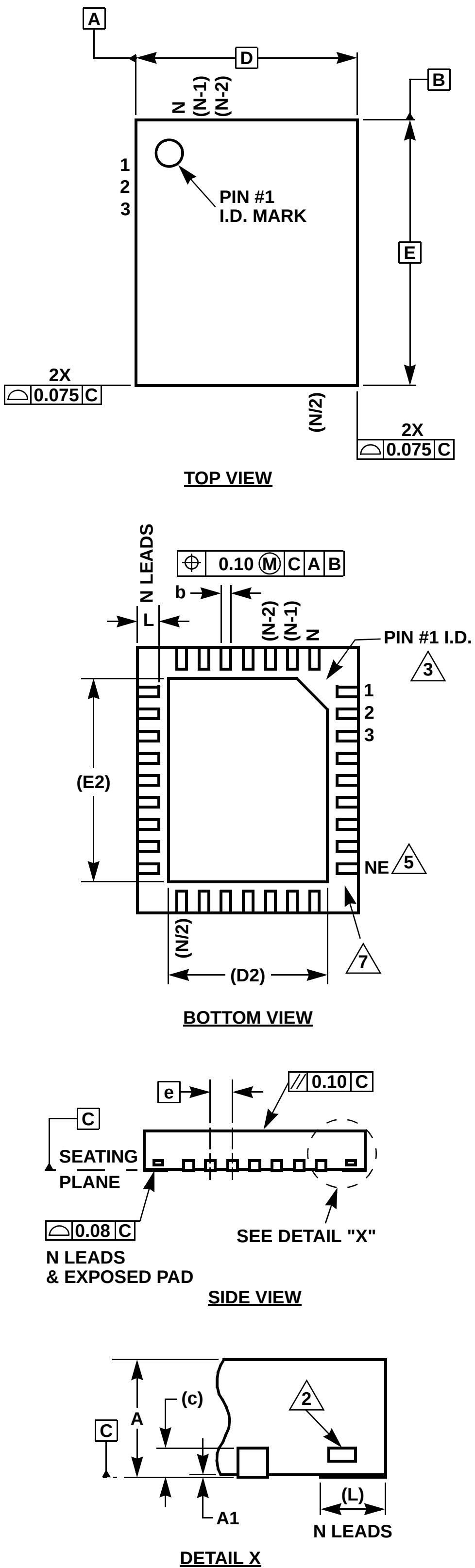
$$R_1 = R_X$$

$$R_2 = R_Z$$

$$R_{SET} = \frac{R_X(R_X + R_Y + R_Z)}{20R_Y}$$

FIGURE 32. EXAMPLE OF THE REPLACEMENT FOR THE MECHANICAL POTENTIOMETER CIRCUIT USING THE EL9200

QFN (Quad Flat No-Lead) Package Family



MDP0046

QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY
(COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS				TOLERANCE	NOTES
	QFN44	QFN38	QFN32			
A	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	+0.03/-0.02	-
b	0.25	0.25	0.23	0.22	±0.02	-
c	0.20	0.20	0.20	0.20	Reference	-
D	7.00	5.00	8.00	5.00	Basic	-
D2	5.10	3.80	5.80	3.60/2.48	Reference	8
E	7.00	7.00	8.00	6.00	Basic	-
E2	5.10	5.80	5.80	4.60/3.40	Reference	8
e	0.50	0.50	0.80	0.50	Basic	-
L	0.55	0.40	0.53	0.50	±0.05	-
N	44	38	32	32	Reference	4
ND	11	7	8	7	Reference	6
NE	11	12	8	9	Reference	5

SYMBOL	MILLIMETERS					TOLER-ANCE	NOTES
	QFN28	QFN24	QFN20		QFN16		
A	0.90	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	0.02	+0.03/ -0.02	-
b	0.25	0.25	0.30	0.25	0.33	±0.02	-
c	0.20	0.20	0.20	0.20	0.20	Reference	-
D	4.00	4.00	5.00	4.00	4.00	Basic	-
D2	2.65	2.80	3.70	2.70	2.40	Reference	-
E	5.00	5.00	5.00	4.00	4.00	Basic	-
E2	3.65	3.80	3.70	2.70	2.40	Reference	-
e	0.50	0.50	0.65	0.50	0.65	Basic	-
L	0.40	0.40	0.40	0.40	0.60	±0.05	-
N	28	24	20	20	16	Reference	4
ND	6	5	5	5	4	Reference	6
NE	8	7	5	5	4	Reference	5

Rev 11 2/07

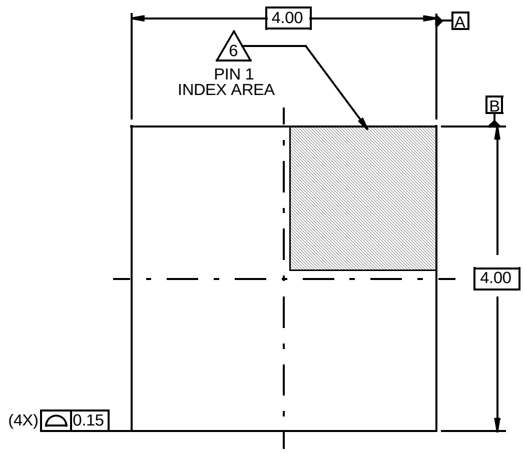
NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.

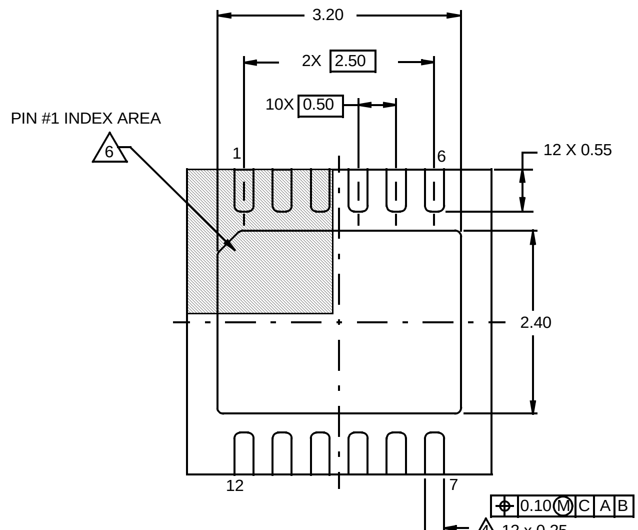
Package Outline Drawing

L12.4x4B

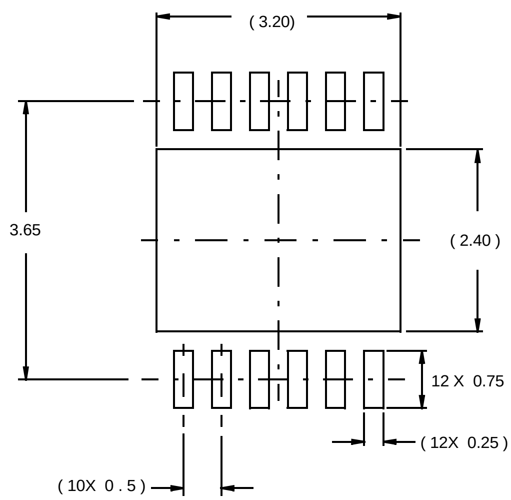
12 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 06/08



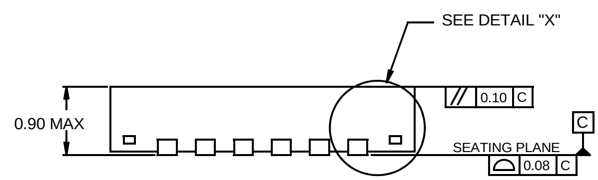
TOP VIEW



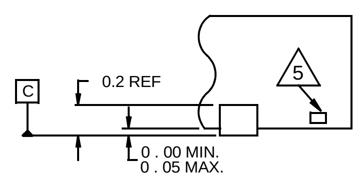
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.